In the Claims:

All of the currently pending claims are listed below including any amendments proposed herein. Please amend the claims as follows:

1. (Currently amended) An amplifier comprising at least one output and first and second supply rails, the amplifier further comprising offset cancellation logic which is operable in a calibration mode to generate a first offset cancellation signal when the at least one output is coupled to a first voltage corresponding to the first supply rail, and a second offset cancellation signal when the at least one output is coupled to a second voltage corresponding to the second supply rail, the offset cancellation logic further being operable to facilitate at least partial cancellation of an offset voltage associated with the at least one output during a normal operation mode using a third offset cancellation signal which substantially corresponds to an average of the first and second offset cancellation signals, wherein the offset cancellation logic comprises a digital-to-analog converter (DAC), a first up/down counter, a second up/down counter, and calibration control logic, the calibration control logic being operable to configure the amplifier for the calibration and normal operation modes, the calibration control logic further being operable during the calibration mode to control the first and second counters and the DAC via one of the counters to generate the first and second offset cancellation signals, the DAC being operable during normal operation mode to generate the third offset cancellation signal.

2. (Original) The amplifier of claim 1 wherein the amplifier comprise one of a switching amplifier topology and a linear amplifier topology.

3. (Original) The amplifier of claim 1 wherein the switching amplifier topology employs continuous-time feedback from the at least one output.

4. (Original) The amplifier of claim 1 wherein the amplifier comprises one of a single-ended amplifier and a differential amplifier.

5. (Original) The amplifier of claim 1 wherein the amplifier comprises multiple channels, each of the channels comprising an instance of the offset cancellation logic.

6. (Original) The amplifier of claim 1 wherein the offset cancellation logic is operable to generate the third offset cancellation signal during the calibration mode.

7. (Original) The amplifier of claim 1 wherein the amplifier comprises a switching differential amplifier, and the at least one output comprises first and second outputs which together form a differential output.

8. (Original) The amplifier of claim 7 wherein the offset cancellation logic is operable to generate the first offset cancellation signal when the first and second outputs are coupled to the first voltage, and the second offset cancellation signal when the first and second outputs are coupled to the second voltage.

Please cancel claim 9 without prejudice.

9. (Canceled)

10. (Original) The amplifier of claim 1 wherein the amplifier is optimized for operation in a frequency range.

11. (Original) The amplifier of claim 10 wherein the frequency range comprises the audio frequency range.

12. (Original) The amplifier of claim 1 further comprising a processor stage and a power output stage, the offset cancellation logic being part of the processor stage.

13. (Original) At least one computer-readable medium having data structures stored therein representative of the processor stage of claim 12.

14. (Original) The at least one computer-readable medium of claim 13 wherein the data structures comprise a simulatable representation of the processor stage.

15. (Original) The at least one computer-readable medium of claim 14 wherein the simulatable representation comprises a netlist.

16. (Original) The at least one computer-readable medium of claim 13 wherein the data structures comprise a code description of the processor stage.

17. (Original) The at least one computer-readable medium of claim 16 wherein the code description corresponds to a hardware description language.

18. (Original) A set of semiconductor processing masks representative of at least a portion of the processor stage of claim 12.

19. (Original) An integrated circuit comprising the offset cancellation logic of claim 1.

20. (Original) An electronic system comprising the integrated circuit of claim 19.

21. (Currently amended) A switching amplifier comprising

a power output stage comprising first and second outputs forming a differential output, and first and second supply rails; and

a processor stage operable to receive an input signal and generate a processed differential signal for amplification by the power output stage, the processor stage further comprising offset cancellation logic which is operable in a calibration mode to generate a first offset cancellation signal when the first and second outputs are coupled to a first voltage corresponding to the first supply rail, and a second offset cancellation signal when the first and second outputs are coupled to a second voltage corresponding to the second supply rail, the offset cancellation logic further being operable to facilitate at least partial cancellation of an offset voltage associated with the different output during a normal operation mode using a third offset cancellation signal which substantially corresponds to an average of the first and second offset cancellation signals, wherein the offset cancellation logic comprises a digital-to-analog converter (DAC), a first up/down counter, a second up/down counter, and calibration control logic, the calibration control logic being operable to configure the amplifier for the calibration and normal operation modes, the calibration control logic further being operable during the calibration mode to control the first and second counters and the DAC via one of the counters to generate the first and second offset cancellation signals, the DAC being operable during normal operation mode to generate the third offset cancellation signal.

Please cancel claim 22 without prejudice.

22. (Canceled)